ABSTRACT OF THE DISCLOSURE

A system-on-chip (SOC) device or a random access memory (RAM) chip includes a RAM block. The RAM block includes memory cells, each of which has three transistors. Each memory cell is coupled to both a read bit line and a write bit line. A transparent continuous refresh mechanism has been implemented to read the content of a memory cell and re-write it back to the memory cell without disturbing the access (read/write) cycle, making refresh operations transparent to the system level. The continuous refresh mechanism includes a collision detection mechanism to prevent writing and reading the same memory cell at the same time.

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